

FIGURE 3

	lode)				1	2	
	Reference (previous r				Time Clot Number	dilina roio-allin	Checksum
e (0001) 400	Msg. Typ Connection Reference (previous node)	address	ddress	IP Address	Interface Number	000	Che
Setup Message (0001) 400		Destination IP address	Source IP Address	Previous Node's IP Address	-Maximum Bandwidth	Dod Dife	Subject of the subjec
	Message Length				Minimum Bandwidth	O	i ga

0010) 500	Connection Reference (condex)	(laning) paring (sering)	Checksum	
Tessage ((Msg. Tvp		# ~	
Setup Success Message (0010) 500	Bandwidth	" " " " " " " " " " " " " " " " " " "	e (own) Rad Bits	
	Message Length	Consocian Defend	Colline Cilori Reference (own)	

FIGURE 5

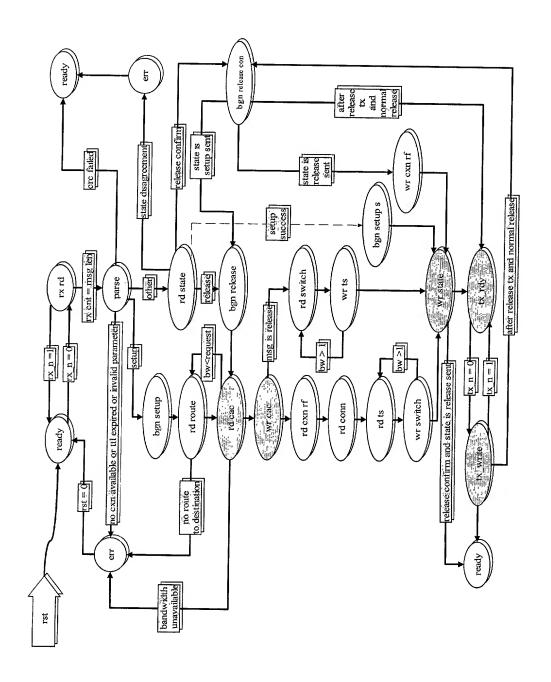


FIGURE 7

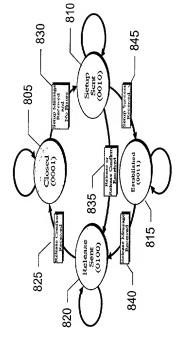


FIGURE 8

OWN CONVECTION REFERENCE RETURN/WATHEN VALUE

INCOMING CHANNEL DENTIFIER

OUTGOING CHANNEL DENTIFIER

INTERFACE

TIME-SLOT Connection Admission Control (CAC) Table 1300
NEXT NODE ADDRESS NEXT NODE INTERFACE* TOTATE BANDWIDTH RETURN VALUE * - - - RETURN VALUE State Table 1000

RETURN/WRITTEN VALUE

PREVIOUS STATE BANDWIDTH PREVIOUS NEXT Connectivity Table 1100 Switch Mapping Table Routing Table 1200 *NOLLAO NEIGHBOR INTERFACE# DESTINATION ADDRESS REQUESTED BANDWIDTH SEQUENTIAL OFFSET (0 to BW-1) , NEIGHBOR ADDRESS OWN CONVECTION REFERENCE OWN CONNECTION REFERENCE ANDEX. FIGURE 12 FIGURE 11 FIGURE 13 FIGURE 10 FIGURE 9

TIME-SLOT

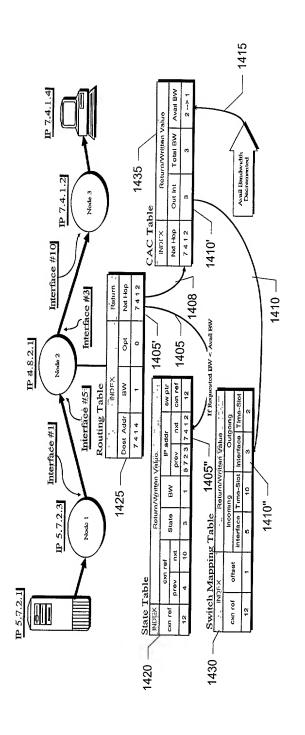


FIGURE 14

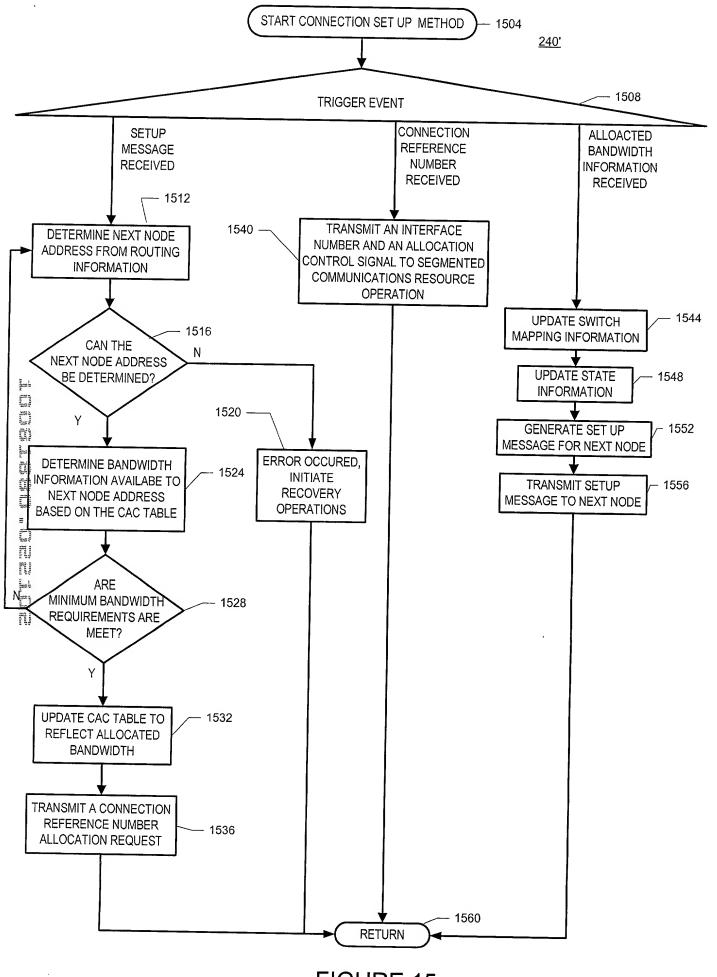


FIGURE 15

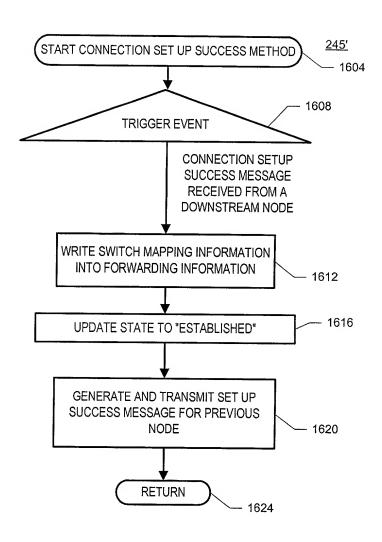


FIGURE 16

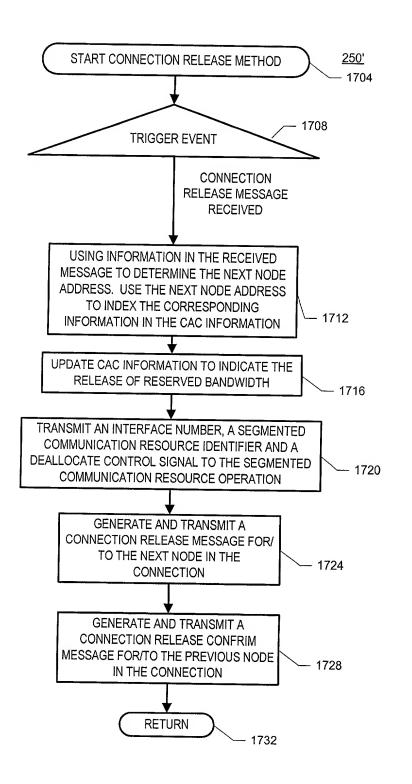


FIGURE 17

FIGURE 18

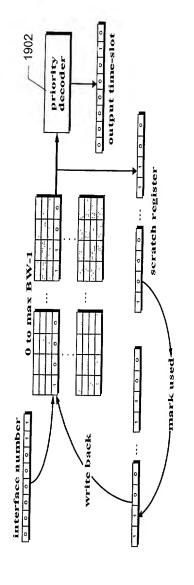


FIGURE 19

1900

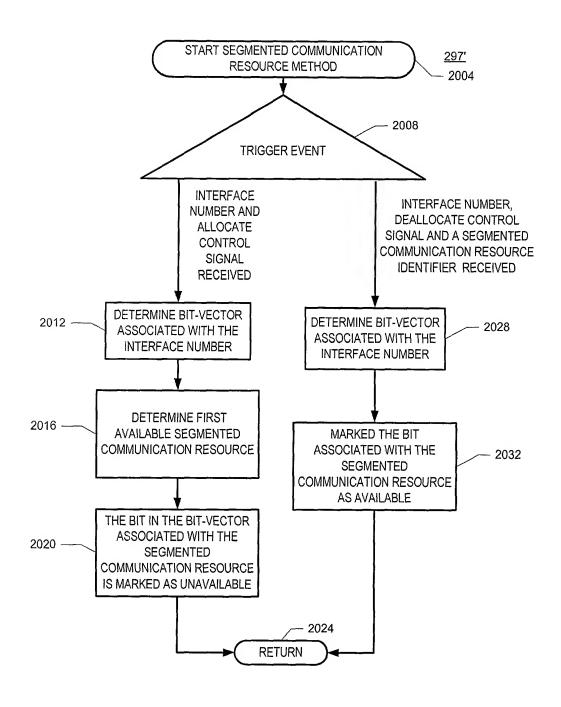


FIGURE 20

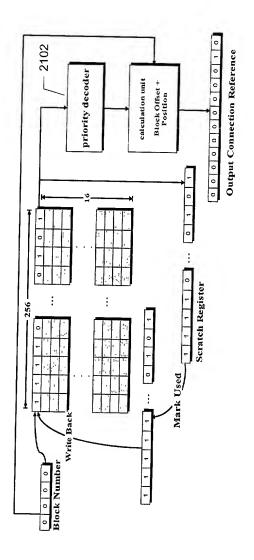
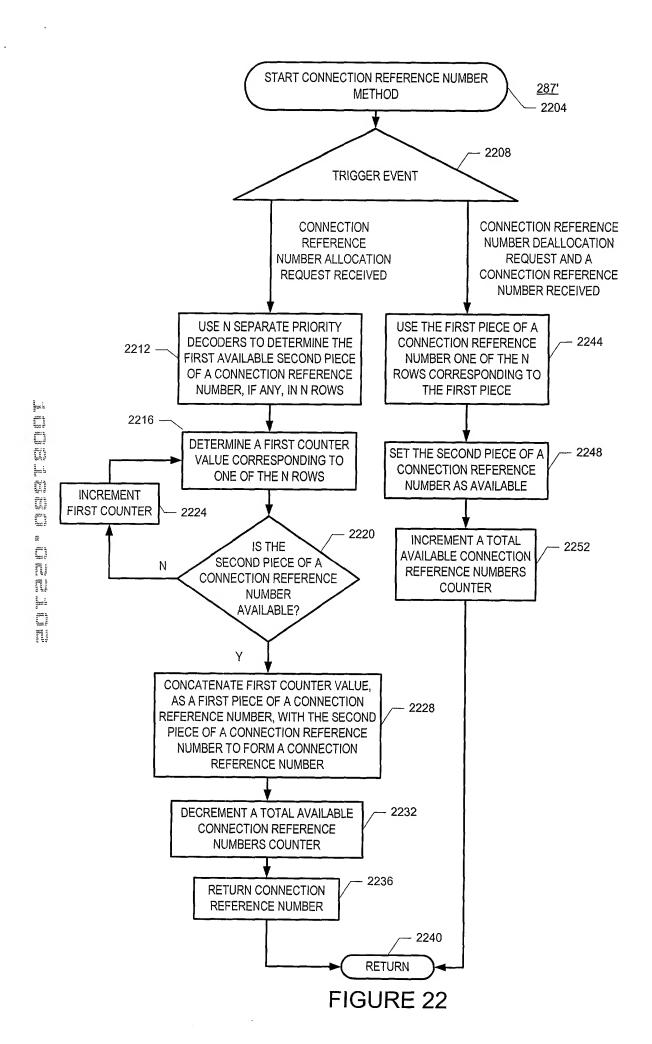


FIGURE 21

2100



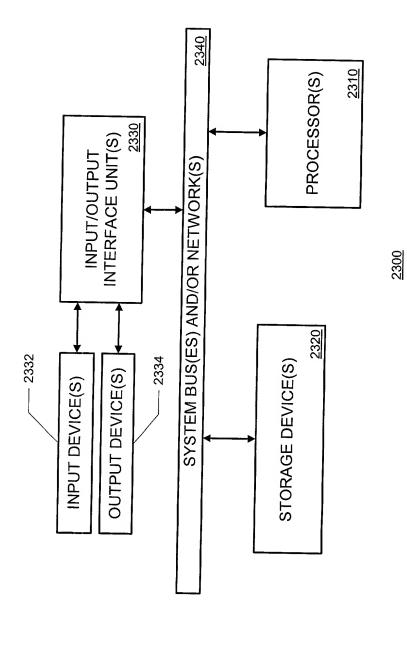


FIGURE 23

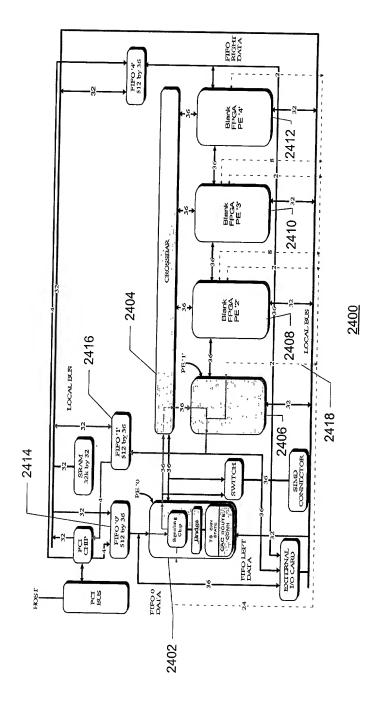


FIGURE 24

	4 0	CAC	NEXT NODE ADDRESS	5-BIT	ZZ00 FIGURE 27	
	9		PPT	-		
	ø		l.			
	^		BANDWIDTH	4-BIT	9	
	8	BLE	BANC	4	2	
	6	AT ON		_		
	10	ROUTING TABLE	RESS		2600 3UR	
	12 11	-	ADDI	Li,	2600 FIGURE 26	
-	13		DEST NODE ADDRESS	5-BIT	L.	
-	14		DEST			
-	ر د					_
-	16		* €E			
-	\exists	_	INTERFACE *	4-BIT	25	
r	18	TABL	2		Ш	
	13	CONNECTIVITY TABLE	RESS	7	2500 FIGURE 25	
	20	NNEC	ADDF		J.	
	21	00	PREVIOUS NODE ADDR	6-BIT	Ε̈́	
L	22		SOCS		_	
[8	Ñ		O. Di	╛		

OWN CONNECTION
REFERENCE
S-BIT (EACH)
S-BIT (EACH)
S-BIT (EACH)
S-BIT (EACH)
S-BIT (EACH)
REFERENCE
S-BIT (EACH)
R

2800

OWN SEQUENTIAL INCOMING CHANNEL IDENTIFIER OUTGOING CHANNEL IDENTIFIER SERFERENCE (0 to BM-1) INTERFACE TIME-SLOT INTERFACE TIME-SLOT

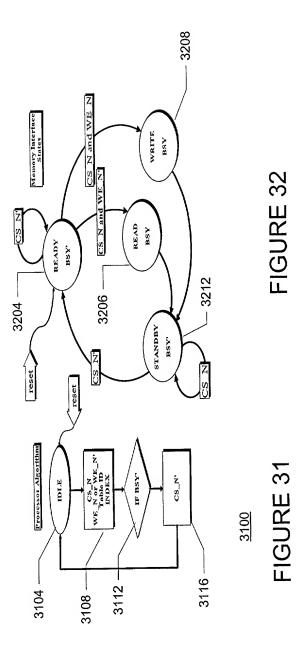
FIGURE 29

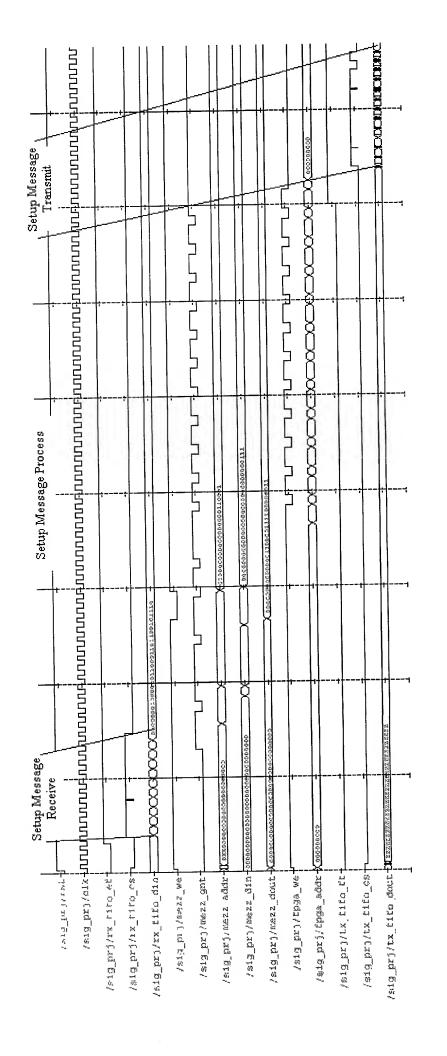
2900

Table 1: Chip Select and Write Enable

No action/High Impedance	-	-
Pause	0	_
Read	1	0
Write	0	0
ACTION	N_3W	CS_N

3000





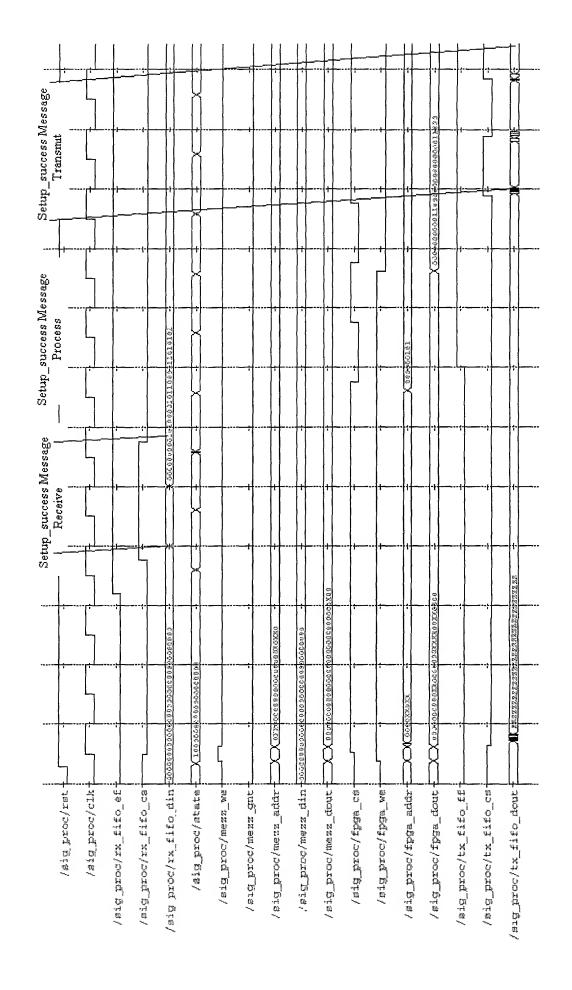


FIGURE 34

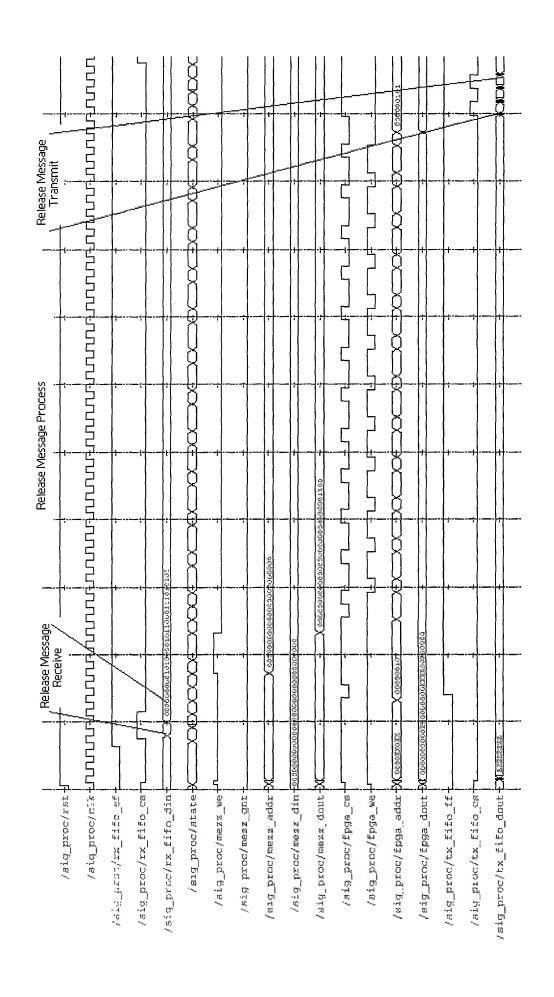


FIGURE 35

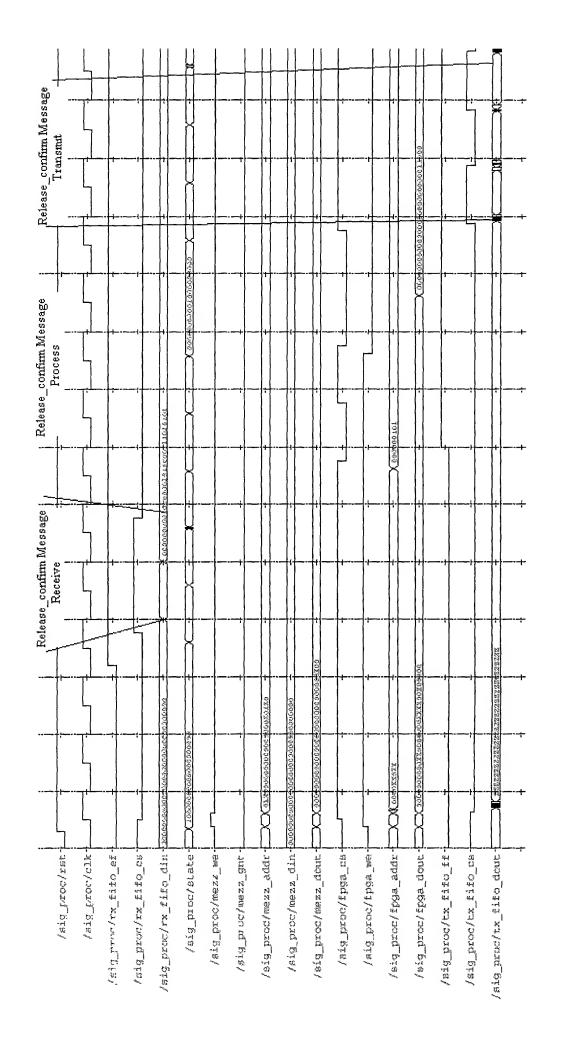


FIGURE 36

Type				Opera	Operations and Cycles	Cycles				Total
								!	ì	
	do	≈	RD route	WR	RD	8	RD TS &	× K	×	7
Setun			& CAC	CAC	Conn	Cxn ref	WR switch	State		- [*] ?
3	cycles	12	8-32	2	4	2	36	-	12	5
									Ì	
400	do	×	RD State					WK State	×	6
saccess	cycles	m	2					1	3	
	Š	λQ	PD State	CS.	RD CAC B	B8	RD Switch &	WR	XΤ	
Dologe	3	<u> </u>		≥ ≥	WR CAC		WR TS	State		21
בובמזכ	cycles	8	2		9		36	1	~	
	č	RX	RD State		>	WR Cxn ref		×	ĭ	,
Dolosco	}	<u> </u>						State		5
confirm	CVCles	m	2			-		-	ო	